SYNCHRONOUS SIGNAL GENERATING METHOD, RECORDING APPARATUS, TRANSMITTING APPARATUS, RECORDING MEDIUM, AND TRANSMISSION MEDIUM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a synchronous signal generating method, recording apparatus, transmitting apparatus, recording medium, and transmission medium in which a p-bit input data word is converted to a q-bit ($q > p$) code word using a plurality of coding tables, and a code word string produced by directly coupling the code words is recorded in a recording medium such as an optical disk and magnetic disk and reproduced, or transmitted via a transmitting portion, in which a coding rate is raised according to high density of recording, a synchronous signal for decoding reproduction data is inserted into every predetermined number of code words in a string of the code words, and the synchronous signal is surely separated from the code word string so as to reproduce digital data with high precision.

2. Description of the Related Art

Generally, a pit length to be recorded in an optical disk has a restriction on a minimum run length (minimum pit or land length) due to optical transmission characteristic for recording and reproducing and physical restraint about pit generation and further, a restriction on a maximum run length (maximum pit or land length) for a reason of facilitation of clock generation. Further for protection of a servo band, and the like, it is necessary to modulate signals to be recorded so that the signals have a suppression characteristic of low-pass components of the signals.

As a conventional modulation method satisfying these

-1-

restrictions, in which the minimum run length (hereinafter referred to also as a minimum reverse interval) is 3T (T = a period of channel bit), and a maximum run length (hereinafter referred to also as a maximum reverse interval) is 11T, an 8 to 14 modulation (EFM) method for use in a compact disk (CD), and EFM+ method for use in a digital versatile disk (DVD) have been well known.

First, in EFM modulation for use in the compact disk (CD), inputted 8-bit (1 byte) digital data is converted to 14-bit run length limited code (hereinafter referred to as a code word) satisfying the run length restriction such that the minimum run length is 3T and the maximum run length is 11T. Furthermore, a 3-bit connection bit for controlling a digital sum value (DSV) and holding a run length restriction rule is attached between the converted code words so that an EFM modulated signal is generated.

In this case, for the minimum run length of 3T, a minimum number of "0" included between logical values "1" and "1" in code words is d=2. On the other hand, for the maximum run length of 11T, a maximum number of "0" included between the logical values "1" and "1" in the code words is k=10. Moreover, the 3-bit connection bit disposed for controlling the DSV and holding the run length restriction rule in order to reduce a DC component and low-pass component of the modulated signal is connected between the 14-bit code words. Thereby, the EFM modulated signal satisfies a run length restriction rule RLL (d, k) = RLL (2, 10) that the minimum run length is 3T and the maximum run length is 11T.

In a CD, the EFM modulated signal with a synchronous signal added is recorded. In a code word string of the EFM modulated signal, a repeating pattern of the maximum run length 11T, that is, a repeating pattern of 11T-11T is avoided so as to set the repeating pattern of 11T-11T as a synchronous signal.

A CD player for reproducing the CD detects the repeating pattern of 11T-11T from signals read from the CD,

thereby sampling the synchronous signal.

Next, in the EFM+ method used for the digital versatile disk (DVD), the inputted 8-bit digital data is converted to a 16-bit code word, these code words are directly coupled to one another without using any connection bit, and thereby 8 to 16 modulation is executed so as to satisfy the run length restriction rule RLL (2, 10) that the minimum run length is 3T and the maximum run length is 11T.

The CD player can, as described above, sample the synchronous signal of the repeating pattern of 11T-11T from signals read from the CD. However, reading information on a recording medium such as an optical disk of much higher density than a DVD or a transmission medium for transmitting modulated signals at higher density would be largely affected by interference between codes. If the synchronous signal used for the CD is used in the medium, the synchronous signal of the repeating pattern of 11T-11T may change to a pattern of 11T-10T or 10T-11T to be read. Conversely, it may occur that a data pattern of 10T-11T or 11T-10T of the EFM modulated signal changes to the repeating pattern of 11T-11T and is erroneously detected as the synchronous signal.

This increases error generation frequency in detecting the synchronous signal in high density recording on a recording medium such as an optical disk or in high density data transmission, leading to easy generation of a burst error due to the loss of synchronization.

Although the DVD using the EFM+ method solves the above problem because the synchronous signal is set at 14T-4T, it causes a lower coding rate.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a synchronous signal generating method, recording apparatus, transmitting apparatus, recording medium, and transmission medium in which a p-bit input data word is converted to a q-bit

(q>p) code word, and a code word string produced by directly coupling the code words is recorded in recording mediums such as an optical disk and magnetic disk and reproduced, or transmitted via a transmitting portion, in which a coding rate is raised according to high density of recording, a synchronous signal for decoding reproduction data is inserted into every predetermined number of code words in a string of the code words, and at the same time, the synchronous signal is surely separated from the code word string so as to reproduce digital data with high precision.

To achieve the object, there is provided a synchronous signal generating method in which a plurality of coding tables is used to subject an input data word of p-bits to modulation and to thereby obtain a code word of q-bits (q>p), the plurality of coding tables storing the code words corresponding to the respective input data words, and state information indicating the coding table for use in modulating a next input data word to obtain a next code word satisfying a predetermined run length restriction rule even with the next code word coupled directly with the code word, and a synchronous signal for decoding reproducing data is inserted into every predetermined number of code words in a string of the code words satisfying the predetermined run length restriction rule, so as to generate a synchronous frame, wherein the synchronous signal is separable from the string of code words satisfying the predetermined run length restriction rule, and comprises a specific code for identifying the position in one sector and a synchronous pattern comprising a first bit pattern of a run length longer than a maximum run length in the predetermined run length restriction rule by 1T or more (T is a period of channel bit of the cord words) and a following second bit pattern of a run length longer than a minimum run length, and the synchronous pattern includes part of a following code word.

In a preferred embodiment of the present invention, a specific coding table and another specific coding table of

-4-

the plurality of coding tables are allotted to have an even/odd relation such that the number of "1" in each of the code words stored corresponding to the respective predetermined input data words is even in the specific coding table and the number of "1" in the code word is odd in the other specific coding table so as to enable a DSV control, and when the predetermined input data word is modulated, the code word having a smaller absolute value is selected from an absolute value of a DSV value obtained from the code word using the specific coding table, and an absolute value of a DSV value obtained from the code word modulated using the other specific coding table, and the DSV control is performed, and a synchronous signal for decoding reproducing data is inserted into every predetermined number of code words in a string of the code words satisfying the predetermined run length restriction rule, so as to generate the synchronous frame.

In a preferred embodiment of the present invention, a plurality of synchronous signal tables is prepared corresponding to the plurality of coding tables, and a plurality of synchronous signal bit patterns for generating the synchronous signal is set in each of the synchronous signal tables, each of the synchronous signal bit pattern having two bit patterns in even/odd relation such that the number of "1" is even in one pattern and is odd in the other pattern to allow selection therebetween by a DSV control.

In a preferred embodiment of the present invention, the p bit is 8 bit, the q bit is 15 bit, and the run length restriction rule sets a minimum run length of a signal of the code words subjected to NRZI conversion at 3T without the synchronous signal and a maximum run length at one of 11T, 12T, 13T and 14T.

Further, in order to achieve the above object, there is provided a recording apparatus in which a plurality of coding tables is used to subject an input data word of p-bits to modulation and to thereby obtain a code word of q-bits

-5-

(q>p), the plurality of coding tables storing the code words corresponding to the respective input data words, and state information indicating the coding table for use in modulating a next input data word to obtain a next code word satisfying a predetermined run length restriction rule even with the next code word coupled directly with the code word, and a synchronous signal for decoding reproducing data is inserted into every predetermined number of code words in a string of the code words satisfying the predetermined run length restriction rule, so as to generate a synchronous frame and sequentially record synchronous frames in a recording medium, wherein the synchronous signal is separable from the string of code words satisfying the predetermined run length restriction rule, and comprises a specific code for identifying the position in one sector and a synchronous pattern comprising a first bit pattern of a run length longer than a maximum run length in the predetermined run length restriction rule by 1T or more (T is a period of channel bit of the cord words) and a following second bit pattern of a run length longer than a minimum run length, and the synchronous pattern includes part of a following code word.

In a preferred embodiment of the present invention, a specific coding table and another specific coding table of the plurality of coding tables are allotted to have an even/odd relation such that the number of "1" in each of the code words stored corresponding to the respective predetermined input data words is even in the specific coding table and the number of "1" in the code word is odd in the other specific coding table so as to enable a DSV control, and when the predetermined input data word is modulated, the code word having a smaller absolute value is selected from an absolute value of a DSV value obtained from the code word using the specific coding table, and an absolute value of a DSV value obtained from the code word modulated using the other specific coding table, and the DSV control is performed, and a synchronous signal for decoding reproducing data is

-6-

inserted into every predetermined number of code words in a string of the code words satisfying the predetermined run length restriction rule, so as to generate the synchronous frame.

5   Further, in order to achieve the above object, there is provided a transmitting apparatus in which a plurality of coding tables is used to subject an input data word of p-bits to modulation and to thereby obtain a code word of q-bits ($q>p$), the plurality of coding tables storing the code words

10   corresponding to the respective input data words, and state information indicating the coding table for use in modulating a next input data word to obtain a next code word satisfying a predetermined run length restriction rule even with the next code word coupled directly with the code word, and a

15   synchronous signal for decoding reproducing data is inserted into every predetermined number of code words in a string of the code words satisfying the predetermined run length restriction rule, so as to generate a synchronous frame and sequentially transmit synchronous frames by wire or radio,

20   wherein the synchronous signal is separable from the string of code words satisfying the predetermined run length restriction rule, and comprises a specific code for identifying the position in one sector and a synchronous pattern comprising a first bit pattern of a run length longer

25   than a maximum run length in the predetermined run length restriction rule by 1T or more (T is a period of channel bit of the cord words) and a following second bit pattern of a run length longer than a minimum run length, and the synchronous pattern includes part of a following code word.

30   In a preferred embodiment of the present invention, a specific coding table and another specific coding table of the plurality of coding tables are allotted to have an even/odd relation such that the number of "1" in each of the code words stored corresponding to the respective

35   predetermined input data words is even in the specific coding table and the number of "1" in the code word is odd in the

-7-

other specific coding table so as to enable a DSV control, and when the predetermined input data word is modulated, the code word having a smaller absolute value is selected from an absolute value of a DSV value obtained from the code word

5   using the specific coding table, and an absolute value of a DSV value obtained from the code word modulated using the other specific coding table, and the DSV control is performed, and a synchronous signal for decoding reproducing data is inserted into every predetermined number of code words in a

10   string of the code words satisfying the predetermined run length restriction rule, so as to generate the synchronous frame.

Further, in order to achieve the above object, there is provided a recording medium which is recorded using the

15   synchronous signal generating method described as the first invention.

Further, in order to achieve the above object, there is provided a transmission medium which is transmitted using the synchronous signal generating method described as the

20   first invention.

The nature, principle and utility of the invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings.

25   BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG.1 is a block diagram showing a disk recording apparatus in an embodiment of a synchronous signal generating

30   method and a recording apparatus according to the present invention;

FIG.2 is a block diagram showing an 8-15 modulator shown in FIG.1;

FIG.3 is a diagram (Diagram 1) showing one example of

35   a coding table;

FIG.4 is a diagram (Diagram 2) showing one example of

the coding table;

FIG.5 is a diagram (Diagram 3) showing one example of the coding table;

FIG.6 is a diagram (Diagram 4) showing one example of

5 the coding table;

FIG.7 is a diagram (Diagram 5) showing one example of the coding table;

FIG.8 is a diagram (Diagram 6) showing one example of the coding table;

10 FIG.9 is a diagram (Diagram 7) showing one example of the coding table;

FIG.10 is a diagram showing a next possible coding table in five classified cases with respect to a plurality of coding tables shown in FIGS.3 to 9;

15 FIG.11 is an explanatory view of replacement between the specific coding table and the other specific coding table among the plurality of coding tables with respect to the input data words;

FIG.12 is a diagram showing one example of a

20 synchronous signal table;

FIG.13 is a diagram showing a format of the coding table of a synchronous signal;

FIG.14 is a diagram showing a format of a transmission signal for one sector;

25 FIG.15 is a flowchart of DSV control at a time of 8-15 modulation; and

FIG.16 is a block diagram showing an information transmitting apparatus in an embodiment of a synchronous signal generating method and a transmitting apparatus

30 according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

One embodiment of a synchronous signal generating

35 method, recording apparatus, transmitting apparatus, recording medium, and transmission medium according to the

present invention will be described in detail with reference to FIGS.1 to 16.

<Synchronous Signal Generating Method, Recording Apparatus, Recording Medium>

5   FIG.1 is a block diagram showing a disk recording apparatus to which one embodiment of the synchronous signal generating method and the recording apparatus according to the present invention are applied.

As shown in FIG.1, a disk recording apparatus 10 to 10 which one embodiment of the synchronous signal generating method and the recording apparatus according to the present invention are applied is roughly constituted of a formatting portion 11, 8-15 modulator 12, and recording driving circuit 13.   In the apparatus, a digital signal relating to 15 information such as image and sound inputted to the disk recording apparatus 10 is subjected to 8-15 modulation by the 8-15 modulator 12 via the formatting portion 11, and the 8-15 modulated signal is recorded in an optical disk or a magnetic disk by the recording driving circuit 13, so that a recording 20 medium 20 according to the present invention is obtained.

First, the digital signal relating to the information such as the image and sound has a continuation of input data words SCt having a bit number $p=8$ bits.   An input data word SCt is inputted together with a control signal to be recorded 25 together into the formatting portion 11, where an error correction code or the like is added and then the format of the data is converted to a control format in accordance with a recording format of the recording medium 20.   Then the 8-bit input data words SCt is outputted as a source cord from the 30 formatting portion 11 to the 8-15 modulator 12.

Subsequently, in the 8-15 modulator 12, a plurality of coding tables described later are referred to, and the input data word SCt having the bit number $p=8$ is converted (8-15 modulated) to a code word having a bit number $q=15$. 35 Additionally, a plurality of synchronous signal tables described later are referred to, thereby a synchronous signal

is inserted into every predetermined number of code words (e.g., 91 code words). Additionally, a code word string constituted of the synchronous signal and a plurality of code words is subjected to NRZI conversion, subsequently

5   subjected to a digital sum value (DSV) control, and outputted as a recording signal to the recording driving circuit 13. Thereafter, as not shown, the recording signal supplied to the recording driving circuit 13 is subjected to optical modulation by an optical modulator, the recording medium 20

10   such as the optical disk and magnetic disk is subsequently irradiated with light via an optical system having an objective lens, and the signal is recorded. In this case, the recording signal obtained as described above is a signal having a coding rate raised with densification to the

15   recording medium 20.

      Here, the 8-15 modulator 12 as a main part of the present invention will be described with reference to FIGS.2 to 15.

      FIG.2 is a block diagram showing the 8-15 modulator

20   shown in FIG.1.

      As shown in FIG.2, the 8-15 modulator 12 as the main part of the present invention is constituted of a code word option presence/absence detector 121, a coding table address computing portion 122 including a plurality of coding tables

25   123, a synchronous frame final data detector 130, a synchronous signal table address computing portion 131 including a plurality of synchronous signal tables 132, an NRZI converter 133, first and second path memories 125, 127, first and second DSV computing memories 124, 126, an absolute

30   value comparing portion 128, and a memory control/recording signal output portion 129.

      Prior to description of an operation of each constituting member in the 8-15 modulator 12, the plurality of coding tables 123 disposed in the coding table address

35   computing portion 122, and the plurality of synchronous signal tables 132 disposed in the synchronous signal table

-11-

address computing portion 131 will first be described.

(Coding Table)

FIGS.3 to 9 are diagrams showing one example of the coding table in order of Diagrams 1 to 7. FIG.10 is a diagram showing a next possible coding table in five classified cases with respect to a plurality of coding tables shown in FIGS.3 to 9. FIG.11 is an explanatory view of replacement between the specific coding table and the other specific coding table among the plurality of coding tables with respect to the input data words.

As shown in FIGS.3 to 9, for the plurality of coding tables 123 disposed in the coding table computing portion 122, an initial table for setting the initial values of choices of the coding tables with respect to the input data word to be first inputted, and six coding tables constituted of states "0" to "5" are prepared beforehand.

Moreover, for the six coding tables, the 8-bit input data word SCt is allotted to "0" to "255" in terms of decimal number, and the respective input data words SCt allotted to "0" to "255" are converted to respective 15-bit code words shown in terms of binary number. Additionally, a right-end number of each code word sets state information (next state) indicating the coding table for use in modulating the input data word SCt in order to obtain a next code word satisfying a predetermined run length restriction rule, even when the code words are directly coupled to each other and thus the code word string is generated. This will be described more concretely. For example, the coding table of state "0" shown in FIG.3 is referred to, and it is then seen that the state information is "4" with input data word "0", the state information is "5" with input data word "1", and the state information is "0" with input data word "2". Therefore, when the coding table of state "0" is used and the input data word "0" is modulated (coded), the coding table of state "4" is used to modulate the next input data word SCt.

Moreover, the six coding tables are set such that each

-12-

inputted data word SCt is converted to a 15-bit code word (one code word) so as to satisfy the run length restriction rule RLL (2, 10) having a minimum run length of 3T and maximum run length of 11T. In this case, as described in the conventional art, with the minimum run length of 3T, d=2 "0"s at minimum are included between logic values "1" and "1" in the 15-bit code word, and with the maximum run length of 11T, k=10 "0"s at maximum are included between the logic values "1" and "1" in the 15-bit code word, so that the run length restriction rule RLL (d, k) = RLL (2, 10) is satisfied. Additionally, the tables are set so as to satisfy the run length restriction rule RLL (2, 10) even with the code word string constituted by directly coupling the code words to each other.

Furthermore, in the six coding tables, as shown in FIG.10, a possible state of the coding table transiting to the next can be classified into five cases of cases 0 to 4 by a zero run length on an LSB side (lower bit side) in the outputted 15-bit code word.

Additionally, for the six coding tables, the code words stored corresponding to the predetermined input data words SCt are allotted to have an even/odd relation such that the number of "1" in 15 bits is even (odd) in the code word in the specific coding table and the number is odd (even) in the code word in the other coding table so as to perform the DSV control. Moreover, the code words are allotted such that during the DSV control of each signal obtained by NRZI conversion of each code word, polarities of DSV values are +- reverse polarities.

Furthermore, as described later, as a mode for switching the code word between the code word of the specific coding table corresponding to the predetermined input data word SCt and the code word of the other coding table corresponding to the same predetermined input data word SCt so that the code word having a smaller absolute value of DSV value (equivalent to a direction in which the DSV value approaches 0) can be taken, the three first to third modes

-13-

are set as described later. Therefore, for the first to third modes described later, it is judged that "there is an option" with respect to the predetermined input data word SCt. In other cases, it is judged that "there is not any option" with respect to the predetermined input data word SCt.

That is, in the first mode, when the specific coding table is the coding table of state "0" and the other specific coding table is the coding table of state "3", the respective signals obtained by NRZI conversion of the respective output code words of the coding tables of states "0" and "3" corresponding to the input data words "0" to "38" have polarities opposite to each other in terms of the DSV value (even/odd parities of the number of "1"s included in the code words are different from each other). However, as shown in a DSV control flowchart at a time of 8-15 modulation of FIG.15 described later, in consideration of a decoding time, when the state information "0" is detected, the respective output code words of the coding table of state "0" corresponding to the input data words "0" to "38" can be replaced with the respective output code words of the coding table of state "3" corresponding to the input data words "0" to "38". Additionally, even when the code words are replaced, the run length restriction rule can be maintained, and further the decoding is possible.

This respect will more concretely be described with reference to section (a) and (b) in FIG.11. As shown in (a) of FIG.11, for example, when the coding table of state "2" is used to convert the input data word "16" to code word {000000001001001}, the coding table of state "0" is designated in accordance with the state information. Thereby, the state information "0" is detected, the coding table of state "0" is used to convert the next inputted data word "6" to code word {000000000100100}, then the number of "1" in the code word {000000000100100} is two and even.

On the other hand, as shown in (b) of FIG.11, when the coding table of state "2" is used to convert the input data

-14-

word "16" to code word {000000001001001}, the next coding
table of state "0" is designated in accordance with the state
information. However, as described above, the table is set
so as to be replaceable with the coding table of state "3".
Thereby, when the coding table of state "3" is used to convert
the input data word "6" to code word {001001000100000}, the
number of "1" in the code word {001001000100000} is three and
odd. Therefore, the coding table of state "0" and the coding
table of state "3" have an even/odd relation of the number
of "1" with respect to the input data word "6".

Thereafter, the code word strings in (a), (b) of FIG.11
is subjected to the NRZI conversion. Here, because the NRZI
conversion carries out modulation by inverting the polarity
at bit "1" while not converting the polarity at bit "0" as
well known, the respective signals are obtained as shown in
(a), (b) of FIG.11.

Thereafter, the DSV values are compared with each other
in order to perform a satisfactory DSV control with respect
to the respective signals obtained by the NRZI conversion of
the code word strings of (a), (b) in FIG.11, and a smaller
absolute value of the DSV value is selected. This DSV value
is an accumulated value from a start point of each signal
obtained by the NRZI conversion with the value of bit "1" as
+1 and the value of bit "0" as -1, as well known. In case
of (a) in Fig.11, the DSV value is +2 while in case of (b)
in Fig.11, the DSV value is -10, so that the polarities of
the DSV values of the two cases are opposite. Also, even if
the coding tables are replaced, the run length restriction
rule can be maintained and further, decoding is possible.
Meanwhile, as for the examples of (a), (b) in Fig.11, because
the case of (a) in Fig.11 provides a smaller absolute value
in terms of the DSV value, this case should be selected.
Usually, the DSV value changes depending on the status since
before.

Next, in the second mode, when the specific coding
table is the coding table of state "2" and the other specific

-15-

coding table is the coding table of state "4", the even/odd
relation is disposed for the number of "1" with respect to
the input data words "0" to "11" and "26" to "47" of the
respective coding tables of states "2" and "4". Also as shown
5   in the DSV control flowchart at the time of 8-15 modulation
of FIG.15, in consideration of the decoding time, when the
state information "2" is detected, the respective output code
words of the coding table of state "2" corresponding to the
input data words "0" to "11" and "26" to "47" can be replaced
10   with the respective output code words of the coding table of
state "4" corresponding to the input data words "0" to "11"
and "26" to "47". Additionally, even when the code words are
replaced, the run length restriction rule can be maintained,
and further the decoding is possible.
15   Subsequently, in the third mode, regarding the coding
table of status "3", when the zero run length on the LSB side
of a previous output code word is 2 to 6 and the input data
word SCt is less than "156", it is also applicable as far as
the run length restriction rule is satisfied even if a next
20   code word is replaced with an output code word in the coding
table of status "0".
In the plurality of coding tables 123 described above,
when the input data word SCt having a bit number p=8 is
converted to the code word having a bit number q=15 bits in
25   accordance with respective promises of the aforementioned
coding time, the 8-15 modulation is performed to satisfy the
run length restriction rule RLL (d, k)=RLL (2, 10) having a
minimum run length of 3T and maximum run length of 11T. This
is not limited. The six coding tables can be used to change
30   the run length restriction rule to RLL (2, 11), RLL (2, 12),
or RLL (2, 13). In this case, when the run length restriction
rule is changed in step 407 of an operation flow (FIG.15)
described later, the minimum run length of 3T and maximum run
length of 12T, 13T, or 14T are partially possible excluding
35   conditions of steps 403, 405.
Of course, when the input data word SCt of p=8 is

-16-

converted to the code word of q=15 bits in the same technical idea as that of the coding table without using the six coding tables, it is also possible to newly set the respective code words and state information in the coding table in order to
5 satisfy the minimum run length of 3T and maximum run length of 12T, 13T, or 14T. When the maximum run length is set to 12T, 13T, or 14T longer than 11T, it is possible to further increase opportunities for the DSV control with an increase of the maximum run length. Additionally, the arrangement of
10 the code words with respect to the data word is not limited to that of the present example, and the arrangement can also be changed without disturbing the run length principle.

(Synchronous Signal Table)

FIG.12 is a diagram showing one example of the
15 synchronous signal table. FIG.13 is a diagram showing a format of the coding table of the synchronous signal. FIG.14 is a diagram showing a format of a transmission signal for one sector.

As shown in FIG.12, for the plurality of synchronous
20 signal tables 132 disposed in the synchronous signal table address computing portion 131, an initial table for setting an initial value of the option of the synchronous signal table with respect to the synchronous signal to be first inputted, and six synchronous signal tables constituted of states "0"
25 to "5" corresponding to the state information of the coding table 123 described above are prepared beforehand.

Moreover, the respective synchronous signal tables of the states "0" to "5" are prepared in accordance with the state information in order to obtain the next code word SCt
30 of final input data of a synchronous frame. Additionally, the signals are grouped into five synchronous signal bit patterns constituted of SY0 to SY5 in each synchronous signal table.

Furthermore, for the five synchronous signal bit
35 patterns SY0 to SY5, two synchronous signal bit patterns constituted of a synchronous signal bit pattern SYn-1t (n is

-17-

in a range of 0 to 5) of 1 to 30 bits on a left side of the drawing and a synchronous signal bit pattern SYn-2t (n is in a range of 0 to 5) of 1 to 30 bits on a right side of the drawing are regarded as one set. For the DSV control, the even/odd relation is disposed such that the number of "1" is even (or odd) in one synchronous signal bit pattern SYn-1t and is odd (or even) in the other synchronous signal bit pattern SYn-2t. The bit patterns are allotted so that the polarities of the DSV values of the respective DSV controlled signals obtained by the NRZI conversion of the respective synchronous signal bit patterns SYn-1t, SYn-2t are +- reverse polarities.

Furthermore, as shown in FIG.13 in an enlarged manner, the synchronous signal bit pattern constituted of 1 to 30 bits is constituted of a specific code of 1 to 13 bits, and a most part of bit strings of a synchronous pattern of 14 to 30 bits following the specific code. Additionally, the synchronous pattern is constituted of 14 to 30 bits in the synchronous signal bit pattern, and a part of the following code word. Moreover, the modulation is performed such that the top bit of the code word SCt following the synchronous signal is set to "1" by setting an uppermost bit as a top bit of the following code word to "1". In this case, for the coding table 123 in which the top bit of the code word is "1", the coding table of state "5" is prepared in the embodiment.

Furthermore, the specific code in the synchronous signal bit pattern is allotted to bits 1 to 13. Therefore, positions in one sector described later can be identified, and DC control is enabled.

Moreover, in the aforementioned synchronous pattern, a first bit pattern having a maximum run length of 13T longer than 11T by 2T in an 8-15 modulation signal is used as a core. The synchronous pattern has a 13T-4T arrangement in which a second bit pattern having a fixed length of 4T is disposed after the first bit pattern of 13T, that is, a bit pattern of {1000000000000010001}, and a fixed pattern common to all the synchronous signals. In this case, the second bit pattern

-18-

of 4T arranged after the first bit pattern of 13T in the synchronous pattern has a fixed length. This is because disposing the specific code in the upper portion of synchronous pattern enables a degree of freedom to increase and also enables the possible number of patterns of the specific code to be sufficiently secured.

Additionally, in the synchronous signal table 132 of the aforementioned embodiment, a maximum interval of the synchronous pattern constituted of bits 14 to 30 in the synchronous signal bit pattern and a part of the following code word has been described in an example of the first synchronous pattern of 13T longer than the maximum run length 11T of the run length restriction rule of the modulation method by 2T. This is not limited. The maximum run length of the first bit pattern may be longer than the maximum run length restriction by 1T or more. The embodiment is effective, particularly when the first bit pattern is longer than the maximum run length by 3T or 4T.

Moreover, the second bit pattern of 4T after the first bit pattern in the synchronous pattern has been described as an example, but this is not limited, and the second bit pattern of 5T or more may be combined. In the embodiment the combination is 13T-4T in consideration of efficiency of the modulation/demodulation method.

Furthermore, as shown in FIG.14, for the synchronous signal according to the synchronous signal bit pattern, any one of synchronous signal bit patterns SY0 to SY5 is selected, for example, for every 91 code words constituting the code word string of the input data word SCt, and added to the top of 91 code words so that the recording signal corresponding to one synchronous frame is outputted. In this case, as shown in FIG.14, for the recording signal format per sector, one sector is constituted of 13 rows, and four synchronous frames are allotted to each row in the column direction. The synchronous signal allotted to each synchronous frame is selected from the synchronous signal bit patterns SY0 to SY5

-19-

shown in FIG.12. For example, the synchronous signal bit pattern allotted to the previous synchronous frame of the first row corresponds to the selected SY0. In and after the first row, the synchronous signal bit pattern allotted to the

5   synchronous frame is structured to cyclically repeat like SY1 to SY3 with a row increase. In this case, a difference among SY1 to SY3 is determined by the aforementioned specific code. That is, one of the respective specific codes of the four synchronous signal bit patterns existing in each row is

10   structured to cyclically repeat in response to the row increase.

Here, turning back to FIG.2, the operation of the 8-15 modulator 12 will be described.

In the 8-15 modulator 12, the synchronous signal and

15   input data word SCt are subjected to the aforementioned DSV control, and the finally outputted synchronous signal and the code word corresponding to the input data word SCt are determined. To facilitate understanding of the description, the DSV control of the input data word SCt will first be

20   described.

When the 8-15 modulator 12 performs the DSV control of the input data word SCt, first the initial coding table (initial value of option of the coding table 123) is selected for the input data word SCt. Subsequently, the 8-bit input

25   data word SCt is inputted, and then the code word option presence/absence detector 121 detects that the output code word corresponding to the present input data word SCt belongs to any one of the first to third modes and has an option for the DSV control, or that the output code word is other than

30   the first to third modes, has no option, and is uniformly determined, based on the present input data word SCt, and the state information determined by the previous output code word (the selected initial value herein) supplied from the coding table address computing portion 122. The detection result

35   is outputted to the coding table address computing portion 122 and absolute value comparing portion 128. Moreover, the

-20-

coding table address computing portion 122 calculates an address of the coding table 123 in accordance with the detection result of "presence of the option" or "absence of the option" from the code word option presence/absence detector 121.

That is, in the first mode, when the state information supplied from the coding table address computing portion 122 is the state "0", and the input data word SCt is "0" to "38", the code word option presence/absence detector 121 outputs the detection result of "presence of the option". In this case, since two addresses are calculated by the coding table address computing portion 122, the coding table 123 outputs two types of code words by a time division processing or the like. Moreover, the coding table address computing portion 122 reads an output code word OC1t corresponding to the input data word SCt of the coding table of state "0" in the coding tables 123 for a path 1, and reads an output code word OC2t corresponding to the input data word SCt of the coding table of state "3" for a path 2.

Moreover, in the second mode, when the state information supplied from the coding table address computing portion 122 is the state "2", and also when the input data word SCt is "0" to "11" or "26" to "47", the code word option presence/absence detector 121 outputs the detection result of "presence of the option". In this case, the coding table address computing portion 122 reads the output code word OC1t corresponding to the input data word SCt of the coding table of state "2" in the coding tables 123 for the path 1, and reads the output code word OC2t corresponding to the input data word SCt of the coding table of state "4" for the path 2.

Furthermore, in the third mode, when the stage information supplied from the coding table address computing portion 122 is the state "3", the zero run length of the previous output code word on the LSB side is in a range of 2 to 6, the input data word SCt is "156" or less, and the coding rule is not broken even with replacement of the next output

-21-

code word with the output code word in the coding table of state "0", the code word option presence/absence detector 121 outputs the detection result of "presence of the option". In this case, the coding table address computing portion 122 reads the output code word OC1t corresponding to the input data word SCt of the coding table of state "3" in the coding tables 123 for the path 1, and reads the output code word OC2t corresponding to the input data word SCt of the coding table of state "0" for the path 2.

On the other hand, the code word option presence/absence detector 121 outputs the detection result of "absence of the option" (uniformly determined) to the coding table address computing portion 122 on conditions other than those of the first to third modes. In this case, the coding table address computing portion 122 calculates only one address, and only the output code word OC1t corresponding to the address is read from the coding table address computing portion 122.

Subsequently, with "the presence of the option" matching the first to third modes, the NRZI converter 133 subjects both the output code words OC1t and OC2t to NRZI conversion. On the other hand, with "the absence of the option" other than the first to third modes, only the output code word OC1t is subjected to the NRZI conversion. In this case, when the each of the code words OC1t, OC2t (with "the presence of the output") or the code word OC1t (with "the absence of the output") outputted from the coding table address computing portion 122 is subjected to the NRZI conversion, either an immediately previous code word OC1t-1 or an immediately previous code word OC2t-1, determined by DSV calculation with respect to the code word (OC1t-1, OC2t-1) immediately before the present word as described later, is stored in an internal memory 133A. Therefore, one immediately previous code word stored in the memory 133A is referred to and thereby to perform the NRZI conversion.

Subsequently, as described later in an operation flow,

-22-

each of the code words OC1t and OC2t-1, or the code word OC1t subjected to the NRZI conversion in the NRZI converter 133 is not immediately stored in the first and second path memories 125, 127. The code word is stored in the first and

5   second path memories 125, 127, after the immediately previous code word is finally determined in accordance with a comparison result of the absolute value of the DSV value with respect to the previous code words calculated in the first and second DSV computing memories 124, 126.

10   Here, the first and second DSV computing memories 124, 126 compute the DSV values (accumulated value) with respect to the previous code words, and the absolute values of the DSV values are compared by the absolute value comparing portion 128. This case will be described. In the first path

15   memory 125, the immediately previous code word OC1t-1, and all the code words determined before the immediately previous code word OC1t-1 are stored in a time series order in an NRZI converted state, and the code words stored in the first path memory 125 in the time series order are outputted to the first

20   DSV computing memory 124. Similarly, in the second path memory 127, the immediately previous code word OC2t-1, and all the code words determined before the immediately previous code word OC2t-1 are stored in the time series order in the NRZI converted state, and the code words stored in the second

25   path memory 127 in the time series order are outputted to the second DSV computing memory 126. Additionally, when nothing is stored in the first and second path memories 125, 127, 0 is regarded, the processing is performed, and then the code words may successively be accumulated.

30   Subsequently, the first DSV computing memory 124 computes the DSV value obtained by adding values over the previous code words and the immediately previous code word OC1t-1, and DSV1t-1 is outputted as the result to the absolute value comparing portion 128. Similarly, the second DSV

35   computing memory 126 computes the DSV value obtained by adding values over the previous code words and the

-23-

immediately previous code word OC2t-1, and DSV2t-1 is outputted as the result to the absolute value comparing portion 128.

Next, the absolute value comparing portion 128 compares a magnitude of an absolute value |DSV1t-1| of the DSV value up to the immediately previous code word OC1t-1 outputted from the first DSV computing memory 124 with that of an absolute value |DSV2t-1| of the DSV value up to the immediately previous code word OC2t-1 outputted from the DSV computing memory 126, and the comparison result is outputted to the memory control/recording signal output portion 129.

Subsequently, when the comparison result sent from the absolute value comparing portion 128 is |DSV1t-1|<|DSV2t-1|, the memory control/recording signal output portion 129 outputs all the previous output code words stored in the first path memory 125, and the immediately previous code word OC1t-1 as the recording signal, and also outputs the signal to the second path memory 127 to rewrite the second path memory 127. Additionally, a storage content of the second DSV computing memory 126 is rewritten into DSV1t-1 which has a smaller absolute value of the DSV value and which is stored in the first DSV computing memory 124.

On the other hand, when the comparison result sent from the absolute value comparing portion 128 is |DSV1t-1|≥|DSV2t-1|, the memory control/recording signal output portion 129 outputs all the previous output code words stored in the second path memory 127, and the immediately previous code word OC2t-1 as the recording signal, and also outputs the signal to the first path memory 125 to rewrite the first path memory 125. Additionally, the storage content of the first DSV computing memory 124 is rewritten into DSV2t-1 which has a smaller absolute value of the DSV value and which is stored in the second DSV computing memory 126.

Therefore, the absolute value comparing portion 128 selects the immediately previous code word which has a smaller absolute value of the DSV value, and a code word

string in which the previous output code words are combined with the selected immediately previous code word is outputted to the recording driving circuit 13 (FIG.1) from the memory control/recording signal output portion 129.

5   Thereafter, with "the presence of the option", the NRZI converter 133 stores the respective signals obtained by the NRZI conversion of the output code words OC1t, OC2t in the first and second path memories 125, 127, respectively. On the other hand, with "the absence of the option", the signal
10   obtained by the NRZI conversion of only the output code word OC1t is stored in both the first and second path memories 125, 127. Accordingly, the respective signals stored in the first and second path memories 125, 127 are immediately before code words OC1t+t, OC2t+1 corresponding to input data word SCt+1
15   to be coded next during the DSV control. Moreover, when the respective signals stored in the first and second path memories 125, 127 are substantially similarly subjected to DSV computing and stored in the first and second DSV computing memories 124, 126, the signals are used in comparing the
20   absolute values of the DSV values during the next operation.

The aforementioned operation is repeated until the input data word SCt is eliminated. After the NRZI conversion, the recording signal which satisfies the run length restriction rule of 3T to 11T and which is DSV controlled can
25   be outputted as the recording signal to the recording medium 20.

On the other hand, the input data word SCt is also inputted into the synchronous frame final data detector 130. The synchronous frame final data detector 130 counts the
30   number of input data words SCt (the synchronous frame is constituted of 91 code words), judges whether or not the input data word SCt is final data of the synchronous frame, and outputs the detection result for inserting the synchronous signal to the synchronous signal table address computing
35   portion 131.

Moreover, when the input data word SCt is detected to

-25-

be the final data of the synchronous frame, and the synchronous signal is inserted, the synchronous signal table address computing portion 131 selects any one of five synchronous signal bit patterns SY0 to SY5 in any one of the synchronous signal tables of states "0" to "5" based on the state information determined by the preceding output code word (the initial value of the initial table herein) supplied from the coding table address computing portion 122 and the information indicating any one of five synchronous signal bit patterns SY0 to SY5 held in the synchronous signal table address computing portion 131. Here, the addresses of two synchronous signal bit patterns SYn-1t, SYn-2t (n is 0 to 5) which correspond to the type selected from SY0 to SY5 and which are different in the even/odd relation from each other are calculated. The synchronous signal table 132 outputs the synchronous signal having two different bit patterns to the NRZI converter 133. Moreover, the NRZI converter 133 subjects two synchronous signals outputted from the synchronous signal table 132 to the NRZI conversion.

Thereafter, by a procedure similar to the procedure with the code word, the absolute values of the DSV values are compared with each other with respect to the immediately previous code word computed by the first and second DSV computing memories 124, 126. After the comparison result of the absolute values of the DSV values is obtained, and the immediately previous code word is determined, two synchronous signals outputted from the NRZI converter 133 are stored in the first and second path memories 125, 127. Moreover, the respective synchronous signals stored in the first and second path memories 125, 127 are subjected to DSV computation and stored in the first and second DSV computing memories 124, 126 similarly as described above, and are used for comparison of the absolute values of the DSV values during the next operation.

In this case, with first insertion of the synchronous signal, it may be assumed that the immediately previous code

word is not stored in the first and second path memories 125, 127.

In this case, at the time when the following input data word SCt results in "the presence of the option" after the synchronous signal is inputted, the absolute values of the DSV values immediately before including the synchronous signal are compared, and the synchronous signal relating with the smaller absolute value of the DSV values immediately before including the synchronous signal is determined. Moreover, the synchronous signal is inserted, for example, into every 91 pieces of word data.

Additionally, the first and second path memories are disposed in the 8-15 modulator 12 in order to temporarily store the synchronous signal and code word string, but the present invention can also be applied even if more path memories are disposed.

A concrete example of the operation will next be described in detail with reference to the DSV control flowchart of the 8-15 modulation time shown in FIG.15, and FIG.2.

First in step 400, the initial tables (the initial values of the option of the synchronous signal table 132 and coding table 123) are selected with respect to the synchronous signal and the input data word SCt.

Subsequently, in step 401, the synchronous signal table address computing portion 131 selects any one of SY0 to SY5 in any one of the synchronous signal tables of states "0" to "5" based on the state determined by the preceding output code word (the selected initial value for the first case) supplied from the coding table address computing portion 122 and the information indicating any one of five synchronous signal bit patterns SY0 to SY5 held in the synchronous signal table address computing portion 131. For example, the synchronous signal bit pattern SYn (n is 0 to 5) in the synchronous signal table of state "n" (n is 0 to 5) is selected. The synchronous signal bit pattern SYn holds

two synchronous signal bit patterns SYn-1t, SYn-2t (n is 0 to 5) whose polarities differ from each other after the NRZI conversion because of the different even/odd relation with respect to the number of "1". Therefore, the NRZI converter 133 converts the two synchronous signal bit patterns SYn-1t, SYn-2t into NRZI, respectively. Thereafter, as described above, the absolute values of the DSV values are compared up to both the immediately previous code words (there is no immediately previous code word with a first synchronous signal), and an either immediately previous code word is determined. Thereafter, two synchronous signals SYn-1t, SYn-2t subjected to the NRZI conversion in the NRZI converter 133 are outputted to the first and second path memories 125, 127, the DSV values including the synchronous signal SYn-1t are computed and stored in the first DSV computing memory 124, and the DSV values including the synchronous signal SYn-2t are computed and stored in the second DSV computing memory 126.

Next in step 402, following the synchronous signal, the 8-bit input data word SCt is inputted.

Subsequently, in steps 403, 405, 407, the code word option presence/absence detecting circuit 121 judges that the present input data word SCt is univocally determined or that there is an option, based on the present input data word SCt, and the state determined by the preceding output code word (the selected initial value for the first case) supplied from the coding table address computing portion 122. The detection result is outputted to the coding table address computing portion 122 and absolute value comparing portion 128.

That is, in step 403, as described in the coding table shown in FIGS.3, 9, the coding tables of states "0" and "3" are noted. According to the first mode, even when the respective output code words of the coding table of state "0" corresponding to the input data words "0" to "38" are replaced with the output code words of the coding table of state "3"

-28-

corresponding to the input data words "0" to "38", the coding rule can be maintained, and the decoding is possible. Therefore, in this step, the code word option presence/absence detecting circuit 121 judges whether or not there is the option according to the first mode.

Moreover, when the state supplied from the coding table address computing portion 122 is "0", and the input data word SCt is "38" or less, namely the condition is matched (Yes), the code word option presence/absence detecting circuit 121 outputs the detection result of "the presence of the option", and the flow shifts to step 404. On the other hand, when the state is not "0", or the input data word SCt is not "38" or less, namely the condition is not matched (No), the flow shifts to step 405.

Subsequently, in step 404, according to the result of "the presence of the option" of step 403, the coding table address computing portion 122 reads the output code word OC1t corresponding to the input data word SCt of the table of state "0" for the path 1 from the coding table 123, and the output code word OC2t corresponding to the input data word SCt of the table of state "3" for the path 2, and the NRZI converter 133 subjects the output code words OC1t, OC2t to the NRZI conversion, respectively.

On the other hand, in step 405, the coding tables of states "2" and "4" are noted from the mismatched result by the step 403. According to the second mode, even when the respective output code words of the coding table of state "2" corresponding to the input data words "0" to "11" and "26" to "47" are replaced with the output code words of the coding table of state "4" corresponding to the input data words "0" to "11" and "26" to "47", the coding rule can be maintained, and the decoding is possible. Therefore, in this step, the code word option presence/absence detecting circuit 121 judges whether or not there is the option according to the second mode.

Moreover, the code word option presence/absence

-29-

detecting circuit 121 judges whether or not the state supplied from the coding table address computing portion 122 is "2", and the input data word SCt is in a range of "11" or less or "26" to "47". When the condition is matched (Yes), the detection result of "the presence of the option" is outputted, and the flow shifts to step 406. On the other hand, when the condition is not matched (No), the flow shifts to step 407.

Subsequently, in step 406, according to the result of "the presence of the option" of step 405, the coding table address computing portion 122 reads the output code word OC1t corresponding to the input data word SCt of the table of state "2" from the coding table 123, and the output code word OC2t corresponding to the input data word SCt of the table of state "4", and the NRZI converter 133 subjects the output code words OC1t, OC2t to the NRZI conversion, respectively.

Subsequently, in step 407, from the mismatched result by the step 405, according to the third mode, with the coding table of state "3", the zero run length of the previous output code word on the LSB side is in a range of 2 to 6 (2 or more is shown in the flow), and the input data word SCt is "156" or less, and even the next output code word is replaced with the output code word in the coding table of state of "0", the coding rule is not broken. In this case, even when the output code word of state "3" is replaced with the output code word of state "0", the coding rule can be maintained, and the decoding is possible. Therefore, in this step, the code word option presence/absence detecting circuit 121 judges whether or not there is the option according to the third mode.

Accordingly, it is judged whether or not the zero run length of the previous output code word on the LSB side is 2 or more, the input data word SCt is "156" or less, the next output code word is selected from the coding table of state "3", and the coding rule is not broken even with replacement with the output code word in the coding table of state "0". When the condition is matched (Yes), the detection result of

-30-

"the presence of the option" is outputted, and the flow shifts to step 408. On the other hand, when the condition is not matched (No), "the absence of the option" can be judged up to this step via the steps 403, 405. Therefore, the detection result of "the absence of the option" is outputted, and the flow shifts to step 409. Additionally, upon judging "the absence of the option" in step 407, without comparing the absolute values of the DSV values or selecting the path, only accumulation into the first and second path memories 125, 127 and DSV calculation updating in the first and second DSV computing memories 124, 126 are performed, until "the presence of the option" results.

In this case, in the embodiment, the run length restriction rule RLL (d, k)=RLL (2, 10) is set to be satisfied in the step 407. When the run length restriction rule RLL (d, k) is changed to RLL (2, 11), RLL (2, 12), or RLL (2, 13) in the step 407, the minimum run length of 3T, and the maximum run length of 12T, 13T, or 14T can partially be realized excluding the conditions of the steps 403, 405.

Subsequently, in step 408, according to the result of "the presence of the option" by the step 407, the coding table address computing portion 122 reads the output code word OC1t corresponding to the input data word SCt of the table of state "3" from the coding table 123, and the output code word OC2t corresponding to the input data word SCt of the table of state "0", and the NRZI converter 133 subjects the output code words OC1t, OC2t to the NRZI conversion, respectively.

Next in step 409, since "the absence of the option" is judged in the step 407, without comparing the absolute values of the immediately previous DSV values, according to the result of "the absence of the option", only the output code word OC1t corresponding to the input data word SCt is read from the coding table 123, the NRZI converter 133 subjects only the output code word OC1t to the NRZI conversion, and the signals obtained by converting only the output code word OC1t into NRZI are stored in both the first and second path

memories 125, 127. In this case, the output code words OC1t, OC2t of the paths 1, 2 have the same value. Thereafter, the flow shifts to step 414, and a processing of steps 414 and 415 is performed.

5   Next in step 410, the respective signals obtained by subjecting the output code words OC1t, OC2t to the NRZI conversion by the NRZI converter 133 in the step 404, 406, or 408 are not stored in the first and second path memories 125, 127. In this state, the absolute values |DSV| of the

10   respective DSV values obtained by subjecting up to the immediately previous code word stored in the first and second DSV computing memories 124, 126 to the DSV computation are compared by the absolute value comparing portion 128. Here, with the code word following the synchronous signal, the

15   absolute values of the respective DSV values computed in the step 401 are compared with each other. With the output code words OC1t, OC2t, the absolute values of the respective DSV values computed by considering up to immediately previous values and stored in step 414 described later at the previous

20   loop are compared with each other.

      Here, when the absolute value |DSV1t-1| of DSV1t-1 from the first DSV computing memory 124 is smaller than the absolute value |DSV2t-1| of DSV2t-1 from the second DSV computing memory 126 (Yes), the previous output code words

25   accumulated in the first path memory 125 are outputted to the second path memory 127 to rewrite the second path memory 127 in step 411. Additionally, the second DSV computing memory 126 is rewritten with DSV1t-1 stored in the first DSV computing memory 124 (the content of the second DSV computing

30   memory 126 is changed to DSV1t-1). On the other hand, when the absolute value |DSV2t-1| of DSV2t-1 from the second DSV computing memory 126 is smaller or the same (No), the previous output code words accumulated in the second path memory 127 are outputted to the first path memory 125 to rewrite the

35   first path memory 125 in step 412. Additionally, the first DSV computing memory 124 is rewritten with DSV2t-1 stored in

the second DSV computing memory 126 (the content of the first DSV computing memory 124 is changed to DSV2t-1).

Subsequently, after the steps 411 and 412, in step 413, the respective signals obtained by subjecting the output code words OC1t, OC2t to the NRZI conversion by the NRZI converter 133, that is, the signal corresponding to the output code word OC1t of the path 1, and the signal corresponding to the output code word OC2t of the path 2 are additionally stored in the first and second path memories 125, 127, respectively.

Subsequently, in step 414, the DSV value including the output code word OC1t of the path 1 is computed and stored in the first DSV computing memory 124, and the DSV value including the output code word OC2t of the path 2 is computed and stored in the second DSV computing memory 126. Here, the respective DSV values stored in the first and second DSV computing memories 124, 126 are used for comparison of the absolute values of the respective DSV values computed by considering up to immediately previous values, in step 410 during the operation steps for the next code word.

Next in step 415, when the synchronous frame final data detector 130 does not judge that the input data word SCt is final data in the synchronous frame (No), then, returning to the step 402, the steps 402 to 415 are repeated. On the other hand, it is judged that the input data word SCt is the final data in the synchronous frame (Yes), and then in step 416 the synchronous signal bit patterns SYn-1t, SYn-2t are subjected to a processing similar to the processing of the steps 410 to 414.

Next in step 417, when inputting of the next input data word SCt does not terminate (No), the flow returns to the step 401. On the other hand, when inputting of the next input data word SCt terminates (Yes), the data string of the output code words stored in the first path memory 125 (or the second path memory 127) is outputted to the recording driving circuit (FIG.1) from the memory control/recording signal output portion 129 in step 418.

-33-

Moreover, for the 15-bit recording signal coded in this manner, the synchronous signal is inserted into every predetermined number of code words (e.g., every 91 code words). The run length restriction rule in which the minimum run length excluding the synchronous signal is 3T (T = period of channel bit) and the maximum run length is 11T is satisfied. The coding rate is raised, and the recording in the recording medium 20 such as the optical disk and magnetic disk at the high density can be realized.

Additionally, the synchronous signal generating method of the present invention is effective in using different DSV control methods. For example, the synchronous signal generating method of the present invention may be applied to a method of not replacing the codes of the tables even if the coding tables in the present embodiment are used, and inserting a DSV control bit for each specific period to perform the DSV control.

<Transmitting apparatus and Medium>

FIG.16 is a block diagram showing an information transmitting apparatus to which one embodiment of a synchronous signal generating method and a transmitting apparatus according to the present invention is applied.

As shown in FIG.16, an information transmitting apparatus 14 to which one embodiment of the synchronous signal generating method and transmitting apparatus according to the present invention is applied is generally constituted of a formatting portion 11, 8-15 modulator 12, and transmitting portion 15. The digital signal relating to the information such as an inputted image and sound is 8-15 modulated by the 8-15 modulator 12 via the formatting portion 11, and the 8-15 modulated signal is transmitted via radio or a cable from the transmitting portion 15, so that a transmission medium 21 according to the present invention is obtained.

In this case, the information transmitting apparatus (transmitting apparatus) 14 is the same as the disk recording

apparatus (recording apparatus) 10 in the formatting portion
11 and 8-15 modulator 12, and is different only in the
transmitting portion 15. Here, during transmission of the
signal 8-15 modulated in the 8-15 modulator 12 in air (radio)

5   or via a transmission cable (wire) from the transmitting
portion 15, when conversion suitable for transmission is
performed in the transmitting portion 15, a small data amount
can be transmitted with a raised coding rate and without any
error.

10   According to the synchronous signal generating method,
recording apparatus, transmitting apparatus, recording
medium, and transmission medium of the present invention as
described above, digital data is held in sectors of a
plurality of synchronous frames at an increased coding rate

15   with a density increased to be transmitted successively, in
which the synchronous frame consists of a synchronous signal
and a code word string satisfying restrictions on minimum run
length and maximum run length, the synchronous signal being
separable from the code word string satisfying the

20   predetermined run length restriction rule and being
constituted with a specific code for identifying the position
in one sector and a synchronous pattern consisting of a first
bit pattern of a run length longer than the maximum run length
of the predetermined run length restriction rule by 1T (T is

25   a period of channel bit of the code word) and a second bit
pattern of a run length longer than the minimum run length,
following the first bit pattern, so that even if each edge
of the signal consisting of the synchronous signal and the
code word string is shifted by 1T due to the effect of

30   interference between codes, both can be identified correctly
to be detected.

        Since the synchronous signal includes a specific code
for identifying the position in a sector and enabling DC
control, if a synchronous signal at the head of a sector

35   cannot temporarily be read on an optical disk of higher
density, or another one is erroneously identified as the

sector head, a correct sector head can be predicted based on a synchronous signal being present thereafter, which enables good reproduction of digital data.

It should be understood that many modifications and adaptations of the invention will become apparent to those skilled in the art and it is intended to encompass such obvious modifications and changes in the scope of the claims appended hereto.